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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/408,429	09/29/1999	MIKLOS SANDORFI	07072/086001	4042

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DALY, CROWLEY & MOFFORD, LLP
SUITE 101
275 TURNPIKE STREET
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EXAMINER

TRAN, DENISE

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 04/20/2004

28

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/408,429

Applicant(s)

SANDORFI, MIKLOS

Examiner

Denise Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 and 19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-17 is/are rejected.
- 7) ☒ Claim(s) 5 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The applicant's amendment filed 1/29/04 has been considered. Claims 1-17 and 19 are presented for examination. Claim 18 has been canceled.

2. **Claims 5 and 19 are objected to** as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, line 4, it is unclear whether "the bi-directional data ports" referred to "a main memory bi-directional data port" and "a plurality of additional bi-directional data ports" or to "a plurality of additional bi-directional data ports" or main memory interface bi-directional ports in claim 1.

As per claim 7, line 4, it is unclear whether "the bi-directional data ports" referred to "a main memory bi-directional data port" and "a plurality of additional bi-directional data ports" or to "a plurality of additional bi-directional data ports" in claim 1.

5. Claims 8-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al., U.S. Patent No. 6,335, 935 (hereinafter Kadambi), in view of Chin et al., U.S. Patent No. 6,356,972, (hereinafter Chin 972).

As per claim 1, Kadambi teaches a processor interface disposed between a memory and a processor (e.g., figs.1-2, el. 10 disposed between els. Processor 52 and memory 12), comprising: a semi conductor integrated circuit having formed therein (e.g., fig. 1, el. switch on chip 10, col. 5, lines 10-15):

a data rebuffering section (e.g., fig. 2, interfaces el. 40, el. 20a, 20c, el. 30a , 30b, el. channel 80 and memory 50) having a memory bi-directional data port (e.g., fig. 2, a bi-directional data port of memory 50 to el. Memory interface 70 which is connected to memory 60 or a bi-directional data port of el. 40 to memory interface 70; col. 5, lines 25-28; col. 7, lines 4-12), a processor bi-directional data port coupled to the processor (e.g., figs. 2 and 16, a bi-directional data port of el. 40 coupled to CPU 52 ; col. 33, lines

5-65), and a plurality of additional bi-directional data ports (e.g., fig. 2, EPIC ports or GPIC ports or EPIC port and GPIC port), such data rebuffering section being adapted to selectively couple data from any one of the plurality of additional bi-directional data ports to the processor bi-directional data port selectively in accordance with a control signal (e.g., col. 26, lines 40-45 and 60-65; col. 28, lines 1-35; col. 12, lines 35-65); and a memory interface (e.g., fig. 2, memory interface 70; col. 7, lines 15-17) having a memory interface bi-directional data port coupled to the memory (e.g., a bi-directional data port of memory interface 70 coupled to memory 60) and an additional memory interface bi-directional data port connected to the memory bi-directional data port of the data rebuffering section (e.g., a bi-direction data port of el. 70 coupled to el. 50 or a bi-directional data port of memory interface 70 coupled to el. 40;), such memory interface providing control signals to the memory (e.g., col. 7, lines 15-25 and col. 13, lines 45-49) and for enabling data transfer between the memory and the processor through the data rebuffering section, as data in such data transfer passes between the additional bi-directional data port of the memory interface and the microprocessor bi-directional data port (e.g., col. 6, lines 45-52; col. 10, lines 10-20; col. 32, lines 15-20, col. 13, lines 45-48; col. 33, lines 5-16 and 60-65). Kadambi does not explicitly show the use of microprocessor, a main memory, microprocessor interface, a main memory port, a microprocessor port, main memory interface port, and a main memory interface for providing control signal to the main memory. Chin 972 shows the use of microprocessor (e.g., fig. 10, el. 12 and col. 10, lines 14-15), a main memory (e.g., col. 7, lines 60-65), and a main memory interface for providing control signal to the main

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memory (e.g., col. 8, lines 55-65); It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Chin 972 into the system of Kadambi because it would increase processing speed by having a central processing unit on a single chip or increase memory space capability and allow managing various connections from/to a microprocessor and a main memory. Also, with respect to a microprocessor interface, a main memory port, a microprocessor port, a main memory interface, the main memory interface port, and an additional main memory interface port, when one of ordinary skill in the art apply the teaching of the microprocessor and main memory of Chin 972 into the system of Kadambi as stated above, the processor interface 10 would be the microprocessor interface; the memory bi-directional data port would be the main memory bi-directional data port; the processor bi-directional data port would be the microprocessor bi-directional data port; the memory interface would be the main memory interface; the memory interface bi-directional data port would be the main memory interface bi-directional data port; the additional memory interface bi-directional data port would be the additional main memory interface bi-directional data port.

As per claim 6, Kadambi shows wherein the data rebuffering section includes: a selector responsive to the control signal for coupling data between a selected one of the bi-directional data ports and the bi-directional data port of the processor (e.g. col. 20, lines 10-20; col. 20, lines 40-55; col. 28, lines 25-35; col. 12, lines 45-55). Kadambi does not explicitly show the use of microprocessor, a main memory, microprocessor

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interface, a main memory port, a microprocessor port, main memory interface port, and a main memory interface for providing control signal to the main memory. Chin 972 shows the use of microprocessor (e.g., fig. 10, el. 12 and col. 10, lines 14-15), a main memory (e.g., col. 7, lines 60-65), and a main memory interface for providing control signal to the main memory (e.g., col. 8, lines 55-65); It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Chin 972 into the system of Kadambi because it would increase processing speed by having a central processing unit on a single chip or increase memory space capability and allow managing various connections from/to a microprocessor and a main memory.

As per claim 7, Kadambi shows wherein the data rebuffering section includes: a selector responsive to the control signal for coupling the bi-directional data port of the processor to either: a selected one of the bi-directional data ports; or the memory, selectively in accordance with the control signal (e.g. col. 20, lines 10-20; col. 20, lines 40-55; col. 28, lines 25-35; col. 12, lines 45-55). Kadambi does not explicitly show the use of microprocessor, a main memory, microprocessor interface, a main memory port, a microprocessor port, main memory interface port, and a main memory interface for providing control signal to the main memory. Chin 972 shows the use of microprocessor (e.g., fig. 10, el. 12 and col. 10, lines 14-15), a main memory (e.g., col. 7, lines 60-65), and a main memory interface for providing control signal to the main memory (e.g., col. 8, lines 55-65); It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Chin 972 into the

system of Kadambi because it would increase processing speed by having a central processing unit on a single chip or increase memory space capability and allow managing various connections from/to a microprocessor and a main memory.

8. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadambi et al., U.S. Patent No. 6,335, 935 (hereinafter Kadambi), in view of Chin et al., U.S. Patent No. 6,356,972, (hereinafter Chin 972) as applied to claim 1 above, and further in view of Stolt et al., U.S. Patent No. 5,721,860 (hereinafter Stolt).

As per claim 2, Kadambi shows the memory is a DRAM (e.g., col. 7, lines 10-12). Kadambi does not explicitly show the use of microprocessor, a main memory, microprocessor interface, a main memory port, a microprocessor port, main memory interface port, and a main memory interface for providing control signal to the main memory. Chin 972 shows the use of microprocessor (e.g., fig. 10, el. 12 and col. 10, lines 14-15), a main memory (e.g., col. 7, lines 60-65), and a main memory interface for providing control signal to the main memory (e.g., col. 8, lines 55-65); and Chin 972 shows the memory is a selected one of a plurality of memory types and one memory type is SDRAM (e.g., col. 3, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Chin 972 into the system of Kadambi because it would increase processing speed by having a central processing unit on a single chip or increase memory space capability and allow managing various connections from/to a microprocessor and a main memory. Kadambi and Chin (972) do not show each type having a different data transfer protocol and

wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide a proper memory protocol to data being transferred between the processor and the memory through the main memory interface. Stolt shows each type having a different data transfer protocol (e.g., abstract) and wherein the main memory interface is configured in accordance with the selected one of the plurality of memory types to provide data being transferred between the processor and the memory through the main memory interface (e.g., abstract; col. 5, line 22 and et seq.); each memory type having a different data transfer protocol and the main memory interface is configured to provide a proper memory protocol to data being transferred (e.g., abstract and col. 2, line 11 and et seq.; col. 5, line 35 and et seq.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Stolt into the combined system of Kadambi and Chin (972) because it would provide an independently controlling of a selected memory type.

As per claim 3, Kadambi shows the memory is a DRAM (e.g., col. 7, lines 10-12); Kadambi does not explicitly show the use of SDRAM. Chin 972 shows the memory is a selected one of a plurality of memory types and one memory type is SDRAM (e.g., col. 3, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Chin 972 into the system of Kadambi because it would provide faster memory operation.

As per claim 4, furthermore, Kadambi, Chin 972 and Stolt do not explicitly show the use of RDRAM. "Official Notice, is taken that both the concept and the advantages of providing RDRAM are well known and expected in the art. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to include a RDRAM because it would provide a high speed memory accessing.

9. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A) Matsumura et al. (U.S. Patent No. 5,410,718) shows a single chip microprocessor having plurality of bi-directional data ports.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications and (703) 746-7240 for Non Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



D.T.
April 17, 2004